IN THE CLAIMS:

Please amend the claims as set forth below.

1-64 (Cancelled)

65. (New) A memory controller comprising:

a first channel control circuit configured to couple to a first channel to access a first memory section;

a second channel control circuit configured to couple to a second channel to access a second memory section, wherein the second channel is independent of and separate from the first channel; and

one or more registers programmable with a first indication of whether or not the first channel and the second channel are interleaved.

66. (New) The memory controller as recited in claim 65 wherein the first indication identifies which portion of an address received by the memory controller is used to select between the first and second channel if the first and second channel are interleaved.

67. (New) The memory controller as recited in claim 65 further comprising a plurality of channel control circuits including the first channel control circuit and the second channel control circuit, wherein the first indication further indicates whether or not other ones of the plurality of channel control circuits are interleaved.

68. (New) The memory controller as recited in claim 65 wherein the first channel includes a plurality of chip select signals, wherein each of the plurality of chip select signals corresponds to a different subsection of the first memory section, and wherein the first channel control circuit is configured to activate one of the plurality of chip select

signals in response to an address received by the memory controller if the address is mapped to the first memory section.

69. (New) The memory controller as recited in claim 68 wherein the one or more registers are programmable with an interleave mode for said subsections.

70. (New) The memory controller as recited in claim 69 wherein the interleave mode is no interleave.

71. (New) The memory controller as recited in claim 69 wherein the interleave mode is interleave of a subset of the subsections and no interleave of remaining ones of the subsections.

72. (New) The memory controller as recited in claim 69 wherein the interleave mode is interleave of the subsections.

73. (New) The memory controller as recited in claim 69 wherein the one or more registers are further programmable with a second indication identifying a second portion of the address that is used to select one of the interleaved subsections.

74. (New) The memory controller as recited in claim 73 wherein the second indication comprises a first bit mask, wherein each bit of the first bit mask corresponds to at least one bit of the address and indicates whether or not the bit of the address is used to select one of the interleaved subsections.

75. (New) The memory controller as recited in claim 68 wherein the second channel includes a second plurality of chip select signals, wherein each of the second plurality of chip select signals corresponds to a different subsection of the second memory section, and wherein the second channel control circuit is configured to activate one of the second plurality of chip select signals in response to the address if the address is mapped to the second memory section.

76. (New) The memory controller as recited in claim 75 wherein the one or more registers are programmable with a second interleave mode for the subsections of the second memory section.

77. (New) The memory controller as recited in claim 76 wherein the second interleave mode differs from the first interleave mode.

78. (New) A system comprising:

a processor configured to transmit an address of a memory location to be accessed; and

a memory controller coupled to receive the address from the processor, wherein the memory controller is configured to couple to a memory including the memory location using at least a first channel and a second channel that is separate from and independent of the first channel, and wherein the memory controller is programmable with a first indication of whether or not the first channel and the second channel are interleaved.

79. (New) The system as recited in claim 78 wherein the first indication identifies which portion of the address received by the memory controller is used to select between the first channel and the second channel if the channels are interleaved.

80. (New) The system as recited in claim 78 wherein the memory controller is further configured to couple to a plurality of separate and independent channels including the first channel and the second channel, wherein the first indication further indicates whether or not other ones of the plurality of channels are interleaved.

81. (New) The system as recited in claim 78 wherein the first channel includes a plurality of chip select signals, wherein each of the plurality of chip select signals

corresponds to a different subsection of a first memory section coupled to the first channel during use, and wherein the memory controller is configured to activate one of the plurality of chip select signals in response to the address if the address is mapped to the first memory section.

82. (New) The system as recited in claim 81 wherein the memory controller is programmable with an interleave mode for said subsections.

83. (New) The system as recited in claim 82 wherein the interleave mode is no interleave.

84. (New) The system as recited in claim 82 wherein the interleave mode is interleave of a subset of the subsections and no interleave of remaining ones of the subsections.

85. (New) The system as recited in claim 82 wherein the interleave mode is interleave of the subsections.

86. (New) The system as recited in claim 82 wherein the memory controller is further programmable with a second indication identifying a second portion of the address that is used to select one of the interleaved subsections.

87. (New) The system as recited in claim 86 wherein the second indication comprises a first bit mask, wherein each bit of the first bit mask corresponds to at least one bit of the address and indicates whether or not the bit of the address is used to select one of the interleaved subsections.

88. (New) The system as recited in claim 81 wherein the second channel includes a second plurality of chip select signals, wherein each of the second plurality of chip select signals corresponds to a different subsection of a second memory section coupled to the second channel during use, and wherein the memory controller is configured to activate

one of the second plurality of chip select signals in response to the address if the address is mapped to the second memory section.

89. (New) The system as recited in claim 88 wherein the memory controller is programmable with an second interleave mode for the subsections of the second memory section.

90. (New) The system as recited in claim 89 wherein the second interleave mode differs from the first interleave mode.